Electronic Version
Stylesheet Version v1.1.1

Vertical Semiconductor Devices

Abstract

A method and structure for increasing the threshold voltage of vertical semiconductor devices. The method comprises creating a deep trench in a substrate whose semiconductor material has an orientation plane perpendicular to the surface of the substrate. Then, vertical transistors are formed around and along the depth of the deep trench. Next, two shallow trench isolation are formed such that they sandwich the deep trench in an active region and the two shallow trench isolation regions abut the active region via planes perpendicular to the orientation plane. Then, the channel regions of the vertical transistors are exposed to the atmosphere in the deep trench and then chemically etched to planes parallel to the orientation plane. Then, a gate dielectric layer is formed on the wall of the deep trench. Finally, the deep trench is filled with poly-silicon to form the gate for the vertical transistors.